19-2652; Rev 0; 10/02

58.6ksps, 14-Bit, 2-Wire Serial ADC in a 14-Pin TSSOP

MAX1069

General Description

The MAX1069 is a low-power, 14-bit successive-approximation analog-to-digital converter (ADC). The device features automatic power-down, an on-chip 4MHz clock, a +4.096V internal reference, and an I²C™-compatible 2-wire serial interface capable of both fast and high-speed modes.

The MAX1069 operates from a single supply and consumes 5mW at the maximum conversion rate of 58.6ksps. AutoShutdown™ powers down the device between conversions, reducing supply current to less than 50µA at a 1ksps throughput rate. The option of a separate digital supply voltage allows direct interfacing with +2.7V to +5.5V digital logic.

The MAX1069 performs a unipolar conversion on its single analog input using its internal 4MHz clock. The full-scale analog input range is determined by the internal reference or by an externally applied reference voltage ranging from 1V to AV_{DD}.

The four address select inputs (ADD0–ADD3) allow up to sixteen MAX1069 devices on the same bus.

The MAX1069 is packaged in a 14-pin TSSOP and offers both commercial and extended temperature ranges. Refer to the MAX1169 for a 16-bit device in a pin-compatible package.

Applications

Hand-Held Portable Applications

Medical Instruments

Battery-Powered Test Equipment

Solar-Powered Remote Systems

Receive Signal Strength Indicators

System Supervision

I²C is a trademark of Philips Corp.
AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Features

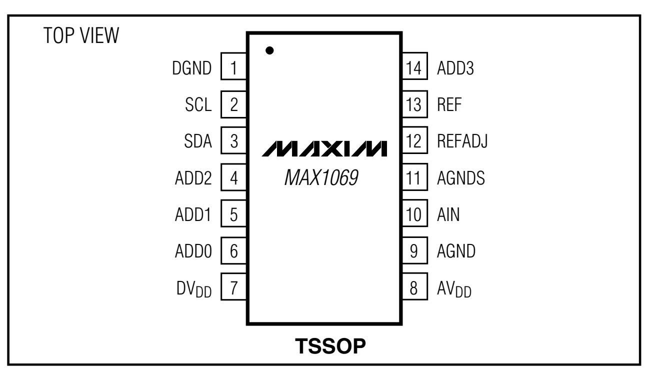
- ♦ **High-Speed I²C-Compatible Serial Interface**
  - **400kHz Fast Mode**
  - **1.7MHz High-Speed Mode**
- ♦ **+4.75V to +5.25V Single Supply**
- ♦ **+2.7V to +5.5V Adjustable Logic Level**
- ♦ **Internal +4.096V Reference**
- ♦ **External Reference: 1V to AV_{DD}**
- ♦ **Internal 4MHz Conversion Clock**
- ♦ **58.6ksps Sampling Rate**
- ♦ **AutoShutdown Between Conversions**
- ♦ **Low Power**
  - **5.0mW at 58.6ksps**
  - **4.2mW at 50ksps**
  - **2.0mW at 10ksps**
  - **0.23mW at 1ksps**
  - **3µW in Shutdown**
- ♦ **Small 14-Pin TSSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1069ACUD	0°C to +70°C	14 TSSOP	±1
MAX1069BCUD	0°C to +70°C	14 TSSOP	±2
MAX1069CCUD	0°C to +70°C	14 TSSOP	±3
MAX1069AEUD*	-40°C to +85°C	14 TSSOP	±1
MAX1069BEUD*	-40°C to +85°C	14 TSSOP	±2
MAX1069CEUD*	-40°C to +85°C	14 TSSOP	±3

**Future product—contact factory for availability.*

Pin Configuration



58.6ksps, 14-Bit, 2-Wire Serial ADC in a 14-Pin TSSOP

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND ....-0.3V to +6V
DV_{DD} to DGND..-0.3V to +6V
AGND to DGND..-0.3V to +0.3V
AGNDS to AGND..-0.3V to +0.3V
AIN, REF, REFADJ to AGND....................-0.3V to (AV_{DD} + 0.3V)
SCL, SDA, ADD_ to DGND......................................-0.3V to +6V
Maximum Current into Any Pin...50mA

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX1069_CUD ....0°C to +70°C
MAX1069_EUD ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +4.75V to +5.25V, DV_{DD} = +2.7V to +5.5V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			14			Bits
Relative Accuracy (Note 2)	INL	MAX1069A			±1	LSB
		MAX1069B			±2	
		MAX1069C			±3	
Differential Nonlinearity	DNL	MAX1069A, no missing codes			±1	LSB
		MAX1069B, no missing codes			±1	
		MAX1069C, no missing codes			±1	
Offset Error				2	5	mV
Offset-Error Temperature Coefficient				1.0		ppm/°C
Gain Error		(Note 3)		±0.25	±0.5	%FSR
Gain Temperature Coefficient				0.1		ppm/°C
DYNAMIC PERFORMANCE ($f_{IN(sine wave)}$ = 1kHz, V_{IN} = $V_{REF(P-P)}$, f_{SAMPLE} = 58.6ksps)						
Signal-to-Noise Plus Distortion	SINAD		81	84		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-99	-86	dB
Spurious-Free Dynamic Range	SFDR		87	102		dB
Signal-to-Noise Ratio	SNR		82	84		dB
Full-Power Bandwidth	FPBW	-3dB point		4		MHz
Full-Linear Bandwidth		SINAD > 81dB		20		kHz
CONVERSION RATE (Figure 11)						
Conversion Time (SCL Stretched Low)	t_{CONV}	Fast mode		7.1	7.5	µs
		High-speed mode		5.8	6	
Throughput Rate (Note 4)	f_{SAMPLE}	Fast mode			19	ksps
		High-speed mode			58.6	
Internal Clock Frequency	f_{CLK}			4		MHz
Track/Hold Acquisition Time	t_{ACQ}	(Note 5)	1100			ns

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +4.75V to +5.25V, DV_{DD} = +2.7V to +5.5V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Aperture Delay (Figure 11c) (Note 6)	t_{AD}	Fast mode		50		ns
		High-speed mode		30		
Aperture Jitter (Figure 11c)	t_{AJ}	Fast mode		100		ps
		High-speed mode		100		
ANALOG INPUT (AIN)						
Input Voltage Range	V_{AIN}		0		V_{REF}	V
Input Leakage Current		On/off-leakage current, V_{AIN} = 0V or AV_{DD}, no clock, f_{SCL} = 0		±0.01	±10	µA
Input Capacitance	C_{IN}			35		pF
INTERNAL REFERENCE (Bypass REFADJ with 0.1µF to AGND and REF with 10µF to AGND)						
REF Output Voltage	V_{REF}		4.056	4.096	4.136	V
Reference Temperature Coefficient	TC_{REF}	T_A = 0°C to +70°C		±20		ppm/°C
		T_A = -40°C to +85°C		±35		
Reference Short-Circuit Current	I_{REFSC}			10	4.136	mA
REFADJ Output Voltage			4.056	4.096	4.000	V
REFADJ Input Range		For small adjustments, from 4.096V		±60		mV
EXTERNAL REFERENCE (REFADJ = AV_{DD})						
REFADJ Buffer Disable Voltage		Pull REFADJ high to disable the internal bandgap reference and reference buffer	AV_{DD} - 0.1			V
REFADJ Buffer Enable Voltage					AV_{DD} - 0.4	V
Reference Input Voltage Range		(Note 7)	1.0		AV_{DD}	V
REF Input Current	I_{REF}	V_{REF} = +4.096V, V_{IN} = $V_{REF(P-P)}$ $f_{IN(sine\ wave)}$ = 1kHz, f_{SAMPLE} = 62.1ksps		27		µA
		V_{REF} = +4.096V, shutdown		0.1		
DIGITAL INPUTS/OUTPUTS (SCL, SDA)						
Input High Voltage	V_{IH}		0.7 × DV_{DD}			V
Input Low Voltage	V_{IL}				0.3 × DV_{DD}	V
Input Hysteresis	V_{HYST}			0.1 × DV_{DD}		V
Input Current	I_{IN}				±10	µA
Input Capacitance	C_{IN}			15		pF
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
ADDRESS SELECT INPUTS (ADD3, ADD2, ADD1, ADD0)						
Input High Voltage			0.7 × DV_{DD}			V
Input Low Voltage					0.3 × DV_{DD}	V
Input Hysteresis				0.1 × DV_{DD}		V
Input Current					±10	µA
Input Capacitance				15		pF

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +4.75V to +5.25V, DV_{DD} = +2.7V to +5.5V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS (AV_{DD}, AGND, DV_{DD}, DGND)							
Analog Supply Voltage	AV_{DD}			4.75		5.25	V
Digital Supply Voltage	DV_{DD}			2.7		5.5	V
Analog Supply Current	I_{AVDD}	Internal reference (powered down between conversions, R/$\overline{W}$ = 0)	f_{SAMPLE} = 58.6ksps		1.8	2.5	mA
			f_{SAMPLE} = 10ksps		0.7		
			f_{SAMPLE} = 1ksps		40		µA
			Shutdown		0.4	5.0	
		Internal reference (always on, R/$\overline{W}$ = 1)	f_{SAMPLE} = 58.6ksps		1.8	2.5	mA
			f_{SAMPLE} = 10ksps		1.4		
			f_{SAMPLE} = 1ksps		1.1		mA
			Shutdown		0.4	5	µA
		External reference (REFADJ = AV_{DD})	f_{SAMPLE} = 58.6ksps		0.90	1.8	mA
			f_{SAMPLE} = 10ksps		0.36		
			f_{SAMPLE} = 1ksps		40		µA
			Shutdown		0.4	5	
Digital Supply Current	I_{DVDD}	f_{SAMPLE} = 58.6ksps			260	400	µA
		f_{SAMPLE} = 10ksps			65		
		f_{SAMPLE} = 1ksps			6		
		Shutdown			0.2	5	
Power-Supply Rejection Ratio	PSRR	AV_{DD} = 5V ±5%, full-scale input (Note 8)			2	6	LSB/V
TIMING CHARACTERISTICS FOR 2-WIRE FAST MODE (Figure 1a and Figure 2)							
Serial Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}			1.3			µs
Hold Time for Start Condition	$t_{HD,STA}$			0.6			µs
Low Period of the SCL Clock	t_{LOW}			1.3			µs
High Period of the SCL Clock	t_{HIGH}			0.6			µs
Setup Time for a Repeated START Condition (Sr)	$t_{SU,STA}$			0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 9)		0		900	ns
Data Setup Time	$t_{SU,DAT}$			100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 10)		20 + $0.1C_B$		300	ns
Fall Time of SDA Transmitting	t_F	(Note 10)		20 + $0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU,STO}$			0.6			µs
Capacitive Load for Each Bus Line	C_B					400	pF
Pulse Width of Spike Suppressed	t_{SP}					50	ns

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +4.75V to +5.25V, DV_{DD} = +2.7V to +5.5V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS FOR 2-WIRE HIGH-SPEED MODE (Figure 1b and Figure 2)						
Serial Clock Frequency	f_{SCLH}	(Note 11)			1.7	MHz
Hold Time, (Repeated) Start Condition	$t_{HD,STA}$		160			ns
Low Period of the SCL Clock	t_{LOW}		320			ns
High Period of the SCL Clock	t_{HIGH}		120			ns
Setup Time for a Repeated START Condition	$t_{SU,STA}$		160			ns
Data Hold Time	$t_{HD,DAT}$	(Note 9)	0		150	ns
Data Setup Time	$t_{SU,DAT}$		10			ns
Rise Time of SCL Signal (Current Source Enabled)	t_{RCL}	(Note 10)	10		80	ns
Rise Time of SCL Signal After Acknowledge Bit	t_{RCL1}	(Note 10)	20		160	ns
Fall Time of SCL Signal	t_{FCL}	(Note 10)	20		80	ns
Rise Time of SDA Signal	t_{RDA}	(Note 10)	20		160	ns
Fall Time of SDA Signal	t_{FDA}	(Note 10)	20		160	ns
Setup Time for STOP Condition	$t_{SU,STO}$		160			ns
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}				10	ns

Note 1: DC accuracy is tested at AV_{DD} = +5.0V and DV_{DD} = +3.0V. Performance at power-supply tolerance limits is guaranteed by power-supply rejection test.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.

Note 3: Offset nullified.

Note 4: One sample is achieved every 18 clocks in continuous conversion mode.

$$f_{SAMPLE} = \left(\frac{18\,\text{clocks}}{f_{SCL}} + t_{CONV}\right)^{-1}$$

Note 5: The track/hold acquisition time is two SCL cycles as illustrated in Figure 11.

$$t_{ACQ} = 2 \times \left(\frac{1}{f_{SCL}}\right)$$

Note 6: A filter on SDA and SCL delays the sampling instant and suppresses noise spikes less than 10ns in high-speed mode and 50ns in fast mode.

Note 7: ADC performance is limited by the converter's noise floor, typically 480µV_{P-P}.

Note 8:

$$PSRR = \frac{\left[V_{FS}(5.25V) - V_{FS}(4.75V)\right] \times \dfrac{2^N}{V_{REF}}}{5.25V - 4.75V}$$

where N is the number of bits (14).

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +4.75V to +5.25V, DV_{DD} = +2.7V to +5.5V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

Note 9: A master device must provide a data hold time for SDA (referred to V_{IL} of SCL) in order to bridge the undefined region of SCL's falling edge (see Figure 1).

Note 10: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 × DV_{DD} and 0.7 × DV_{DD}.

Note 11: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

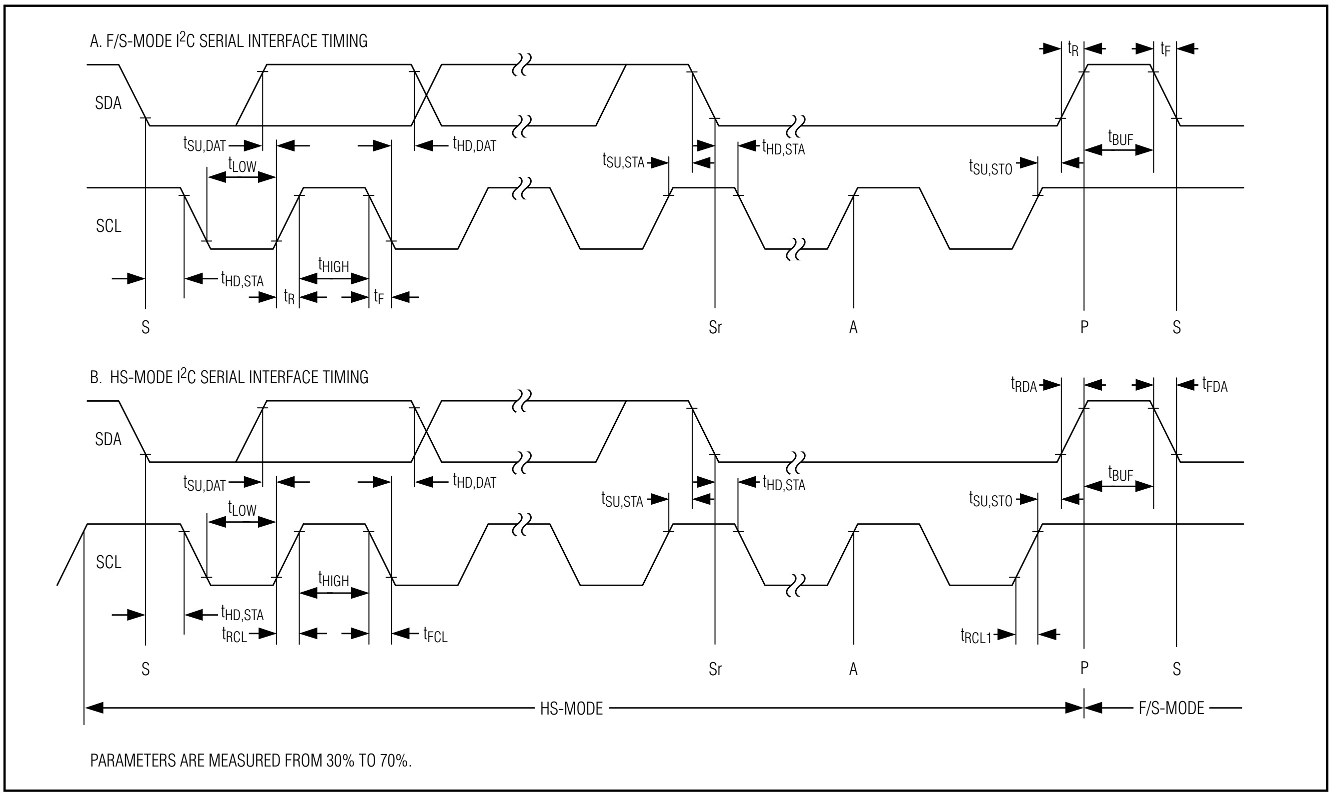


Figure 1. I²C Serial Interface Timing

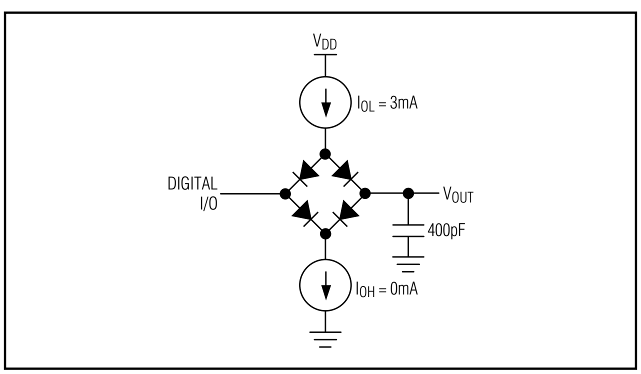
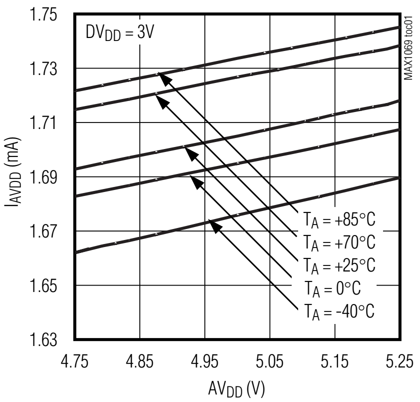


Figure 2. Load Circuit

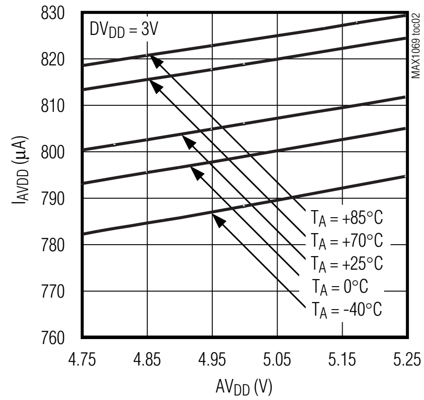
Typical Operating Characteristics

(DV_{DD} = +3.0V, AV_{DD} = +5.0V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = +25°C, unless otherwise noted.)

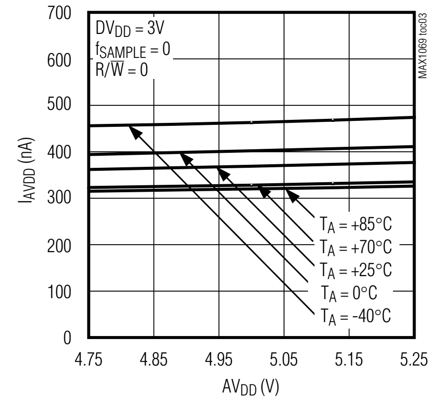
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (INTERNAL REFERENCE)



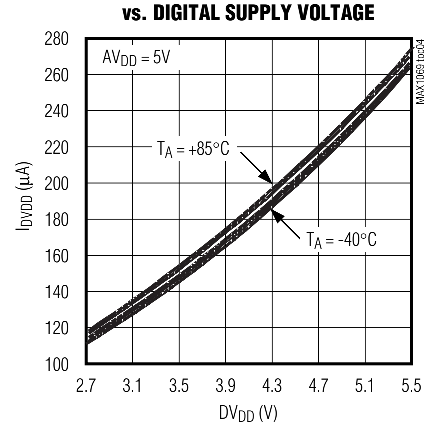
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (EXTERNAL REFERENCE)



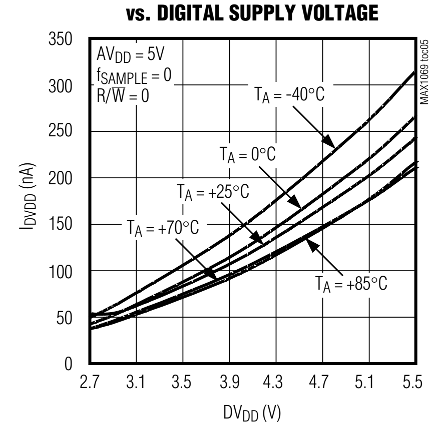
ANALOG SHUTDOWN CURRENT vs. ANALOG SUPPLY VOLTAGE



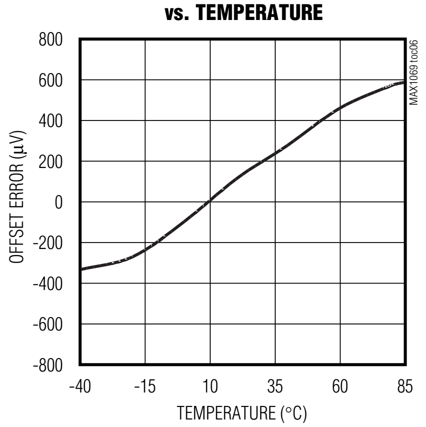
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



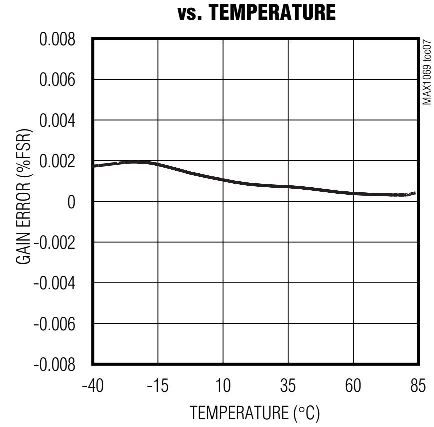
DIGITAL SHUTDOWN CURRENT vs. DIGITAL SUPPLY VOLTAGE



OFFSET ERROR vs. TEMPERATURE



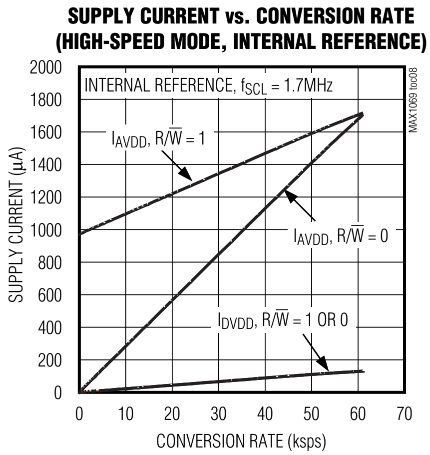
GAIN ERROR vs. TEMPERATURE

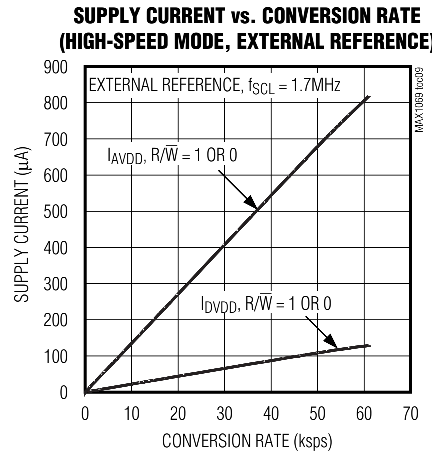


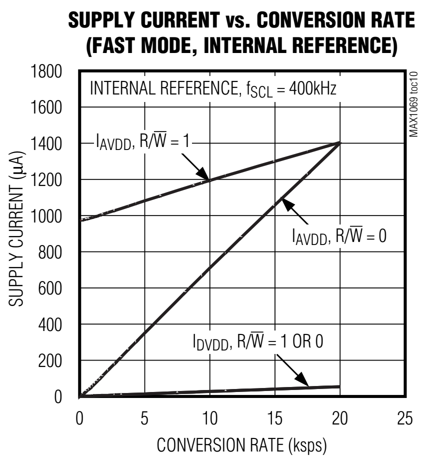
58.6ksps, 14-Bit, 2-Wire Serial ADC in a 14-Pin TSSOP

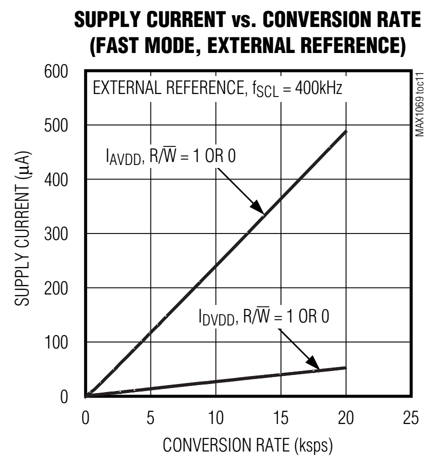
Typical Operating Characteristics (continued)

(DV_{DD} = +3.0V, AV_{DD} = +5.0V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = +25°C, unless otherwise noted.)





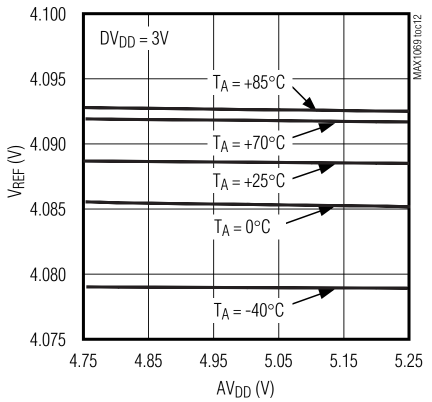




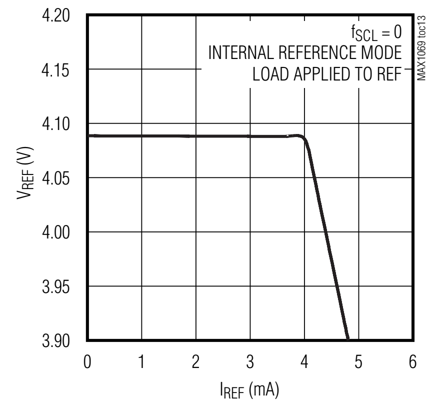
Typical Operating Characteristics (continued)

(DV_{DD} = +3.0V, AV_{DD} = +5.0V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = +25°C, unless otherwise noted.)

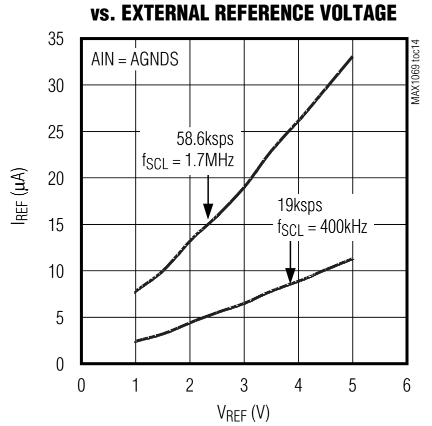
INTERNAL +4.096V REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



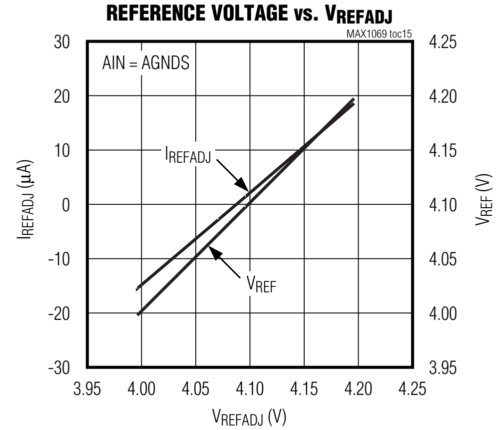
INTERNAL REFERENCE VOLTAGE vs. REF LOAD



EXTERNAL REFERENCE CURRENT vs. EXTERNAL REFERENCE VOLTAGE



EXTERNAL REFERENCE CURRENT AND REFERENCE VOLTAGE vs. V_{REFADJ}

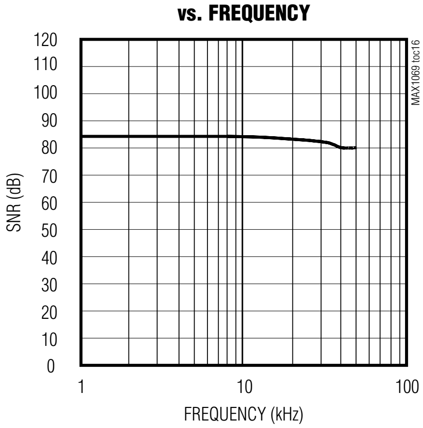


58.6ksps, 14-Bit, 2-Wire Serial ADC in a 14-Pin TSSOP

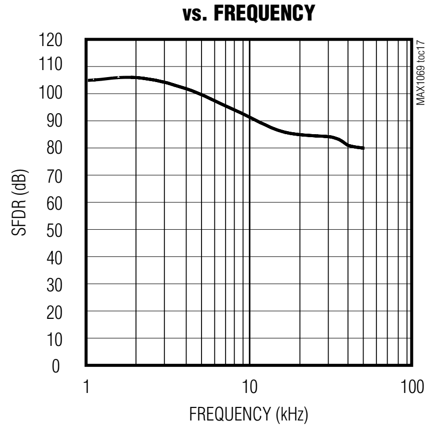
Typical Operating Characteristics (continued)

(DV_{DD} = +3.0V, AV_{DD} = +5.0V, f_{SCL} = 1.7MHz (33% duty cycle), f_{SAMPLE} = 58.6ksps, V_{REF} = +4.096V, external reference applied to REF, REFADJ = AV_{DD}, C_{REF} = 10µF, T_A = +25°C, unless otherwise noted.)

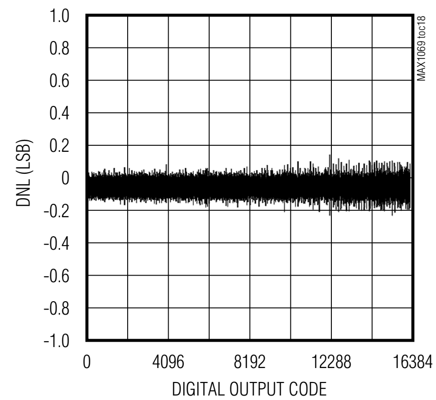
SIGNAL-TO-NOISE RATIO vs. FREQUENCY



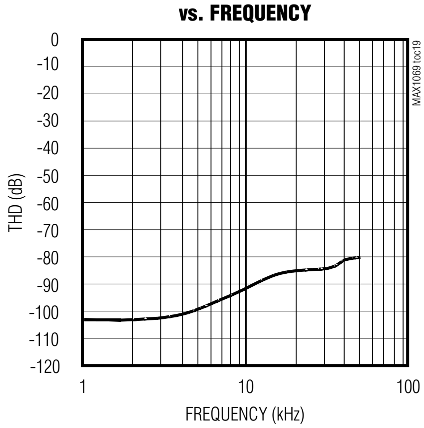
SPURIOUS-FREE DYNAMIC RANGE vs. FREQUENCY



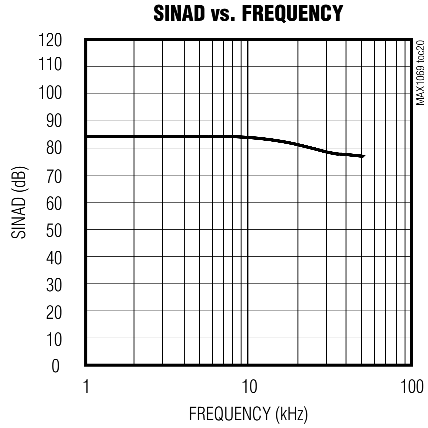
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



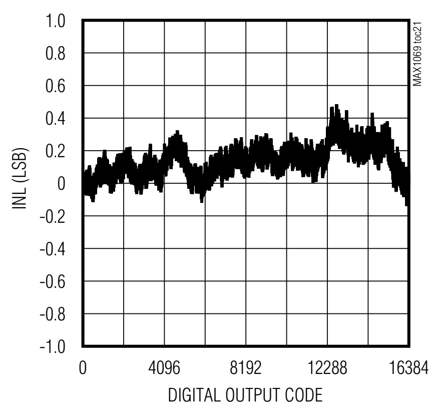
TOTAL HARMONIC DISTORTION vs. FREQUENCY



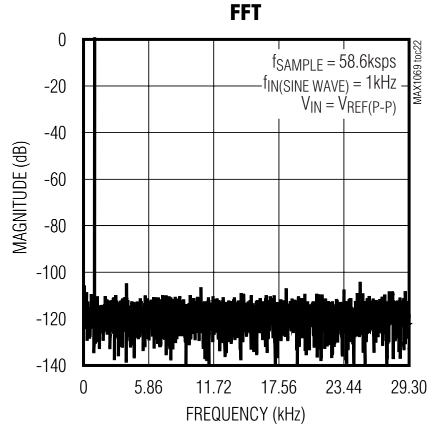
SINAD vs. FREQUENCY



INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



FFT



Pin Description

PIN	NAME	FUNCTION
1	DGND	Digital Ground
2	SCL	Clock Input
3	SDA	Data Input/Output
4	ADD2	Address Select Input 2
5	ADD1	Address Select Input 1
6	ADD0	Address Select Input 0
7	DV_{DD}	Digital Power Input. Bypass to DGND with a 0.1µF capacitor.
8	AV_{DD}	Analog Power Input. Bypass to AGND with a 0.1µF capacitor.
9	AGND	Analog Ground
10	AIN	Analog Input
11	AGNDS	Analog Signal Ground. Negative reference for analog input. Connect to AGND.
12	REFADJ	Internal Reference Output and Reference Buffer Input. Bypass to AGND with a 0.1µF capacitor. Connect REFADJ to AV_{DD} to disable the internal bandgap reference and reference-buffer amplifier.
13	REF	Reference Buffer Output and External Reference Input. Bypass to AGND with a 10µF capacitor when using the internal reference.
14	ADD3	Address Select Input 3

Detailed Description

The MAX1069 analog-to-digital converter (ADC) uses successive-approximation conversion (SAR) techniques and on-chip track-and-hold (T/H) circuitry to capture and convert an analog signal to a serial 14-bit digital output.

The MAX1069 performs a unipolar conversion on its single analog input using its internal 4MHz clock. The full-scale analog input range is determined by the internal reference or by an externally applied reference voltage ranging from 1V to AV_{DD}.

The flexible 2-wire serial interface provides easy connection to microcontrollers (µCs) and supports data rates up to 1.7MHz. Figure 3 shows the simplified functional diagram for the MAX1069 and Figure 4 shows the typical application circuit.

Power Supply

To maintain a low-noise environment, the MAX1069 provides separate analog and digital power-supply inputs. The analog circuitry requires a +5V supply and consumes only 900µA at sampling rates up to 58.6ksps. The digital supply voltage accepts voltages from +2.7V to +5.5V to ensure compatibility with low-voltage ASICs. The MAX1069 wakes up in shutdown mode when power is applied irrespective of the AV_{DD} and DV_{DD} sequence.

Analog Input and Track/Hold

The MAX1069 analog input contains a track-and-hold (T/H) capacitor, T/H switches, comparator, and a switched capacitor digital-to-analog converter (DAC) (Figure 5).

As shown in Figure 11c, the MAX1069 acquisition period is the two clock cycles prior to the conversion period. The T/H switches are normally in the hold position. During the acquisition period the T/H switches are in the track position and $C_{T/H}$ charges to the analog input signal. Before a conversion begins, the T/H switches move to the hold position retaining the charge on $C_{T/H}$ as a sample of the analog input signal.

During the conversion interval, the switched capacitive DAC adjusts to restore the comparator input voltage to zero within the limits of 14-bit resolution. This is equivalent to transferring a charge of 35pF × (V_{AIN} - V_{AGNDS}) from $C_{T/H}$ to the binary-weighted capacitive DAC,

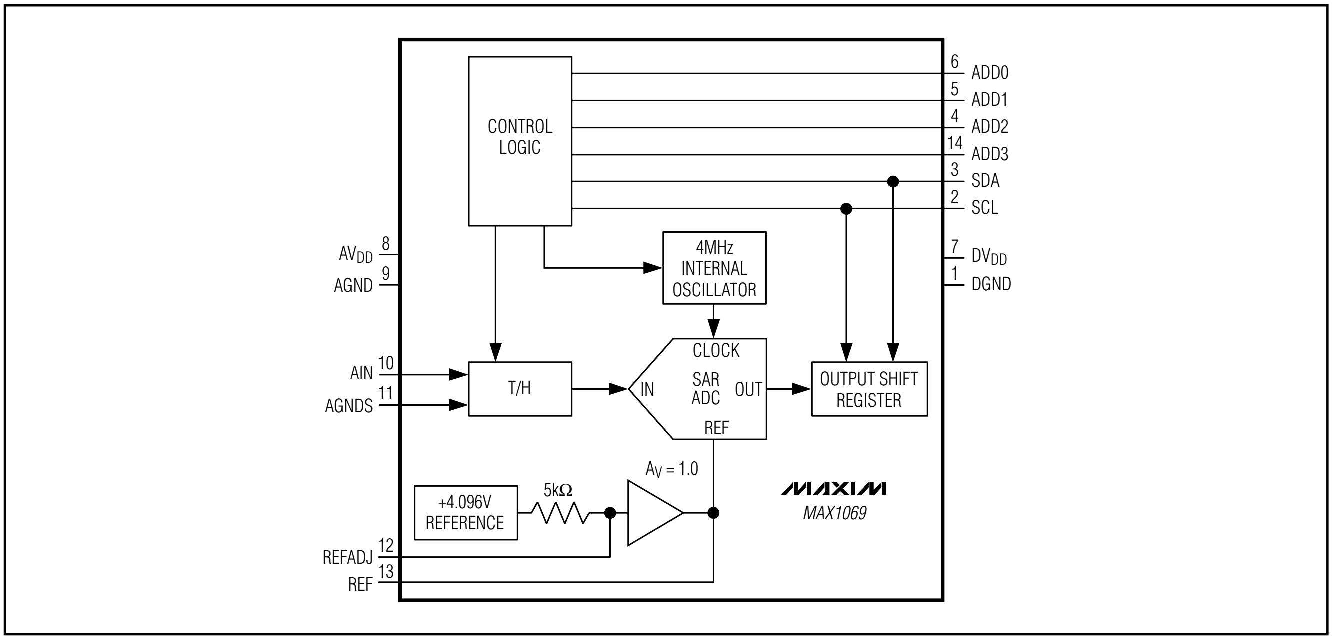


Figure 3. MAX1069 Simplified Functional Diagram

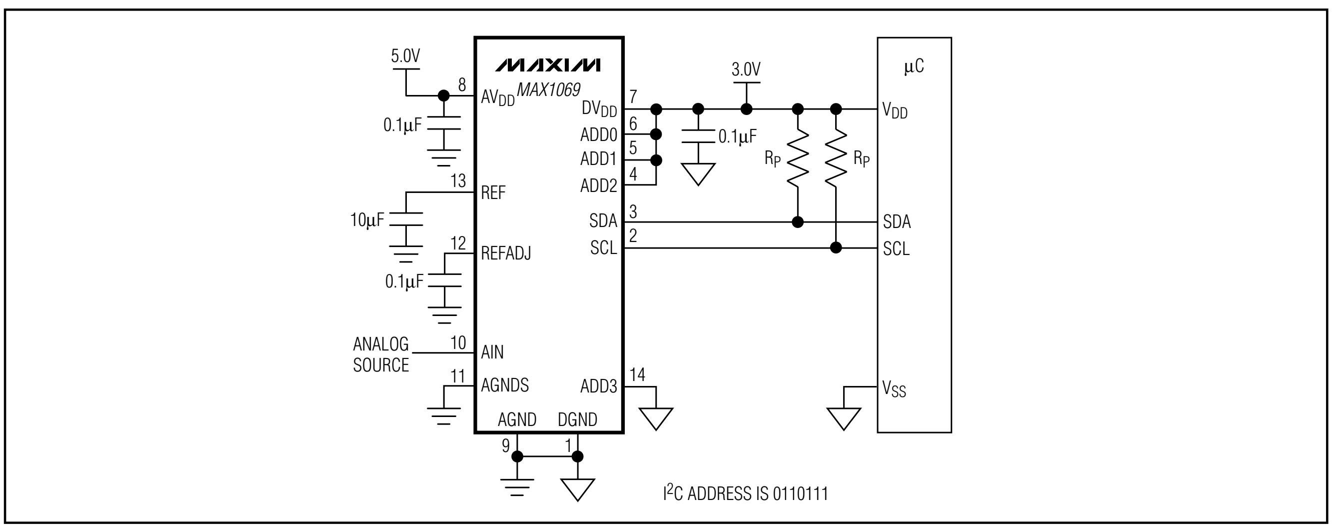


Figure 4. Typical Application Circuit

forming a digital representation of the analog input signal. During the conversion period, the MAX1069 holds SCL low (clock stretching).

The time required for the T/H to acquire an input signal is a function of the analog input source impedance. If the input signal source impedance is high, lengthen the acquisition time by reducing f_{SCL}. The MAX1069 provides two SCL cycles (t_{ACQ}), in which the track-and-hold capacitance must acquire a charge representing the input signal. Minimize the input source impedance (R_{SOURCE}) to allow the track-and-hold capacitance to charge within the allotted time. R_{SOURCE} should be less than 12.9kΩ for f_{SCL} = 400kHz and less than 2.4kΩ for f_{SCL} = 1.7MHz. R_{SOURCE} is calculated with the following equation:

$$R_{SOURCE} \le \frac{2}{f_{SCL} \times \ln(2 \times 2^N) \times C_{IN}} - R_{IN}$$

where R_{SOURCE} is the analog input source impedance, f_{SCL} is the maximum system SCL frequency, N is 14 (the number of bits of resolution), C_{IN} is 35pF (the sum of $C_{T/H}$ and input stray capacitance), and R_{IN} is 800Ω (the T/H switch resistances).

To improve the input-signal bandwidth under AC conditions, drive AIN with a wideband buffer (>4MHz) that can drive the ADC's input capacitance and settle quickly (see the *Input Buffer* section).

An RC filter at AIN reduces the input track-and-hold switching transient by providing charge for $C_{T/H}$.

Analog Input Bandwidth

The MAX1069 features input-tracking circuitry with a 4MHz small-signal bandwidth. The 4MHz input bandwidth makes it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Use anti-alias filtering to avoid high-frequency signals being aliased into the frequency band of interest.

Analog Input Range and Protection

Internal ESD (electrostatic discharge) protection diodes clamp AIN, REF, and REFADJ to AV_{DD} and AGNDS/AGND (Figure 6). These diodes allow the analog inputs to swing from (AGND - 0.3V) to (AV_{DD} + 0.3V) without causing damage to the device. For accurate conversions, the inputs must not go more than 50mV beyond their rails.

If the analog inputs exceed 300mV beyond their rails, limit the current to 2mA.

Internal Clock

The MAX1069 contains an internal 4MHz oscillator that drives the SAR conversion clock. During conversion, SCL is held low (clock stretching). An internal register stores data when the conversion is in progress. When the MAX1069 releases SCL, the master reads the conversion results at any clock rate up to 1.7MHz (Figure 11).

Digital Interface

The MAX1069 features an I^2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX1069 and the master at rates up to 1.7MHz. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL.

SDA and SCL require pullup resistors (500Ω or greater, Figure 4). Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. Nine clock cycles are required to transfer the data into or out of the MAX1069. The data on SDA must remain stable during the high period of the SCL clock pulse as changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high.

START and STOP Conditions

The master initiates a transmission with a START condition (S), a high-to-low transition on SDA with SCL high. The master terminates a transmission with a STOP condition (P), a low-to-high transition on SDA while SCL is high (Figure 7). The STOP condition frees the bus and places all devices in F/S mode (see the *Bus Timing* section). Use a repeated START condition (Sr) in place

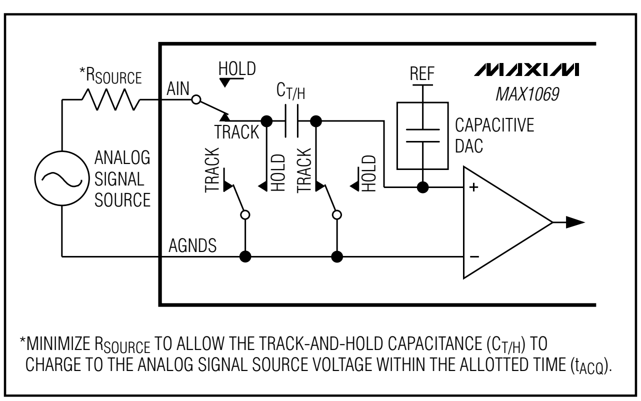


Figure 5. Equivalent Input Circuit

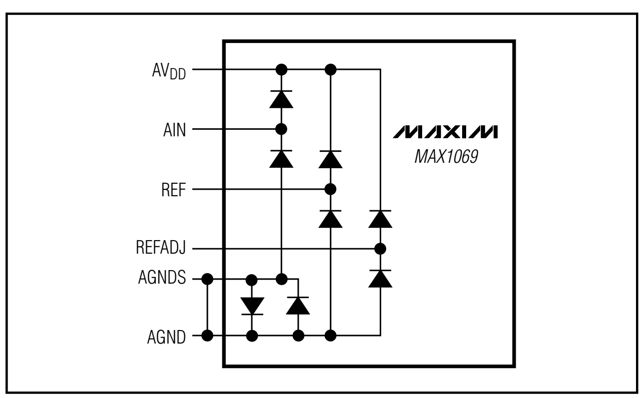


Figure 6. Internal Protection Diodes

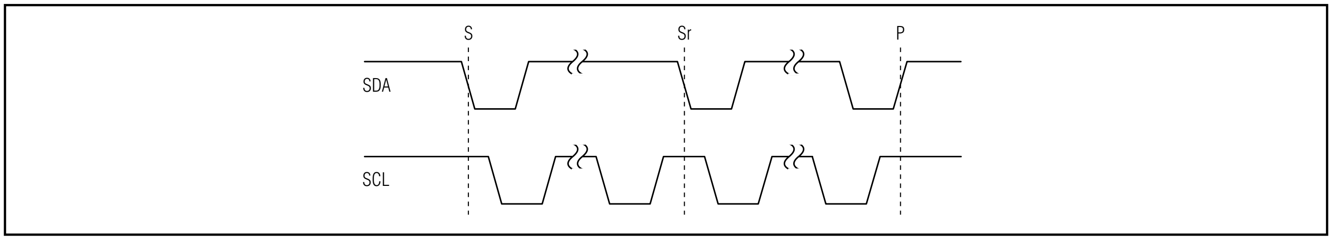


Figure 7. START and STOP Conditions

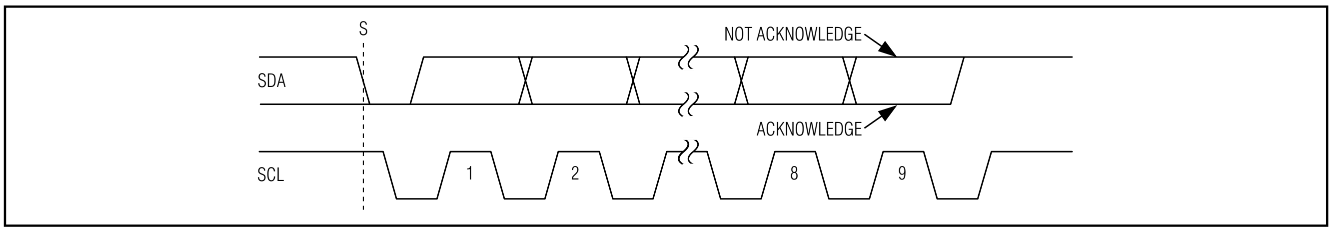


Figure 8. Acknowledge Bits

of a STOP condition to leave the bus active and in its current timing mode (see the *HS-Mode* section).

Acknowledge Bits

Successful data transfers are acknowledged with an acknowledge bit (A) or a not-acknowledge bit ($\overline{A}$). Both the master and the MAX1069 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 8). To generate a not acknowledge, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

Slave Address

A master initiates communication with a slave device by issuing a START condition followed by a slave address byte. As shown in Figure 9, the slave address byte consists of 7 address bits and a read/write bit (R/$\overline{W}$). When idle, the MAX1069 continuously waits for a START condition followed by its slave address. When the MAX1069 recognizes its slave address, it acquires the analog input signal and prepares for conversion. The first three bits (MSBs) of the slave address have been factory programmed and are always **011**. Connecting ADD3–ADD0 to DV_{DD} or DGND, programs the last four bits (LSBs) of the slave address high or low.

Since the MAX1069 does not require setup or configuration, the least significant bit (LSB) of the address byte (R/$\overline{W}$) controls power-down. In external reference mode (REFADJ = AV_{DD}), R/$\overline{W}$ is a don't care. In internal reference mode, setting R/$\overline{W}$ = 1 places the device in normal operation and setting R/$\overline{W}$ = 0 powers down the internal reference following the conversion (see the *Internal Reference Shutdown* section).

After receiving the address, the MAX1069 (slave) issues an acknowledge by pulling SDA low for one clock cycle.

Bus Timing

At power-up, the MAX1069 bus timing defaults to fast mode (F/S-mode), allowing conversion rates up to 19ksps. The MAX1069 must operate in high-speed mode (HS-mode) to achieve conversion rates up to 58.6ksps. Figure 1 shows the bus timing for the MAX1069 2-wire interface.

HS-Mode

At power-up, the MAX1069 bus timing is set for F/S-mode. The master selects HS-mode by addressing all devices on the bus with the HS-mode master code 0000 1XXX (X = don't care). After successfully receiving the HS-mode master code, the MAX1069 issues a not acknowledge allowing SDA to be pulled high for one

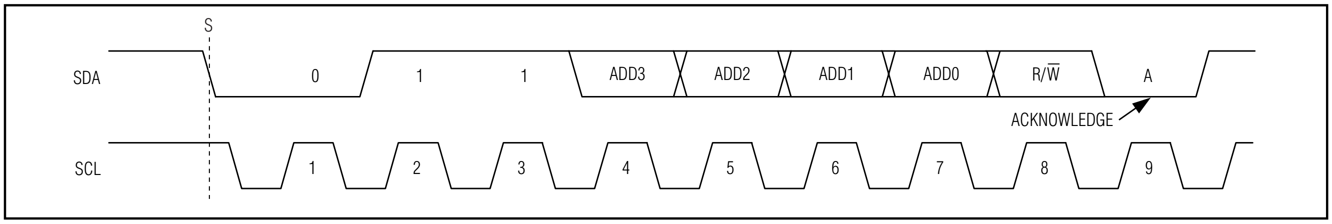


Figure 9. MAX1069 Slave Address Byte

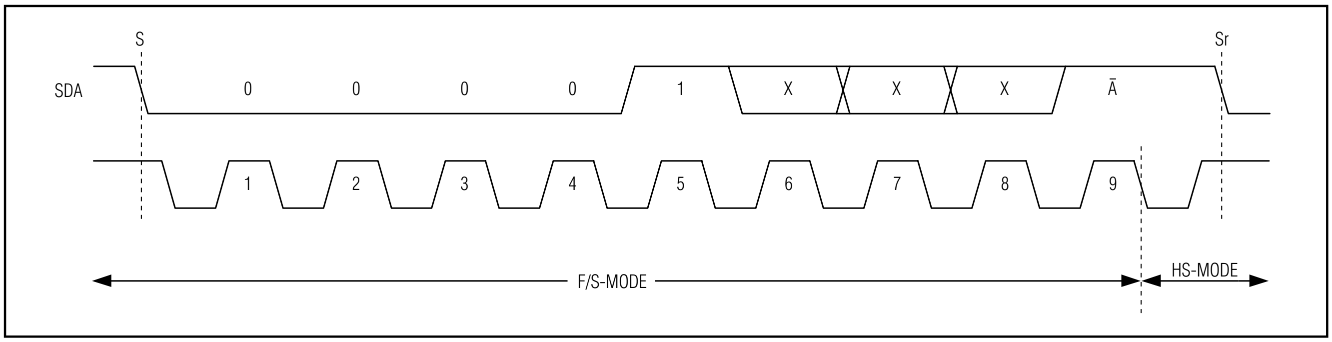


Figure 10. F/S-Mode to HS-Mode Transfer

clock cycle (Figure 10). After the not acknowledge, the MAX1069 is in HS-mode. The master must then send a repeated START followed by a slave address to initiate HS-mode communication. If the master generates a STOP condition, the MAX1069 returns to F/S-mode.

Data Byte (Read Cycle)

Initiate a read cycle to begin a conversion. A read cycle begins with the master issuing a START condition followed by seven address bits and a read bit (R/$\overline{W}$). The standard I²C-compatible interface requires that R/$\overline{W}$ = 1 to read from a device, however, since the MAX1069 does not require setup or configuration, the read mode is inherent and R/$\overline{W}$ controls power-down (see the *Internal Reference Shutdown* section). If the address byte is successfully received, the MAX1069 (slave) issues an acknowledge and begins conversion.

As seen in Figure 11, the MAX1069 holds SCL low during conversion. When the conversion is complete, SCL is released and the master can clock data out of the device. The most significant byte of the conversion is available first and contains D13 to D6. The least significant byte contains D5 to D0 plus two trailing sub bits S1 and S0. Data can be continuously converted as long as the master acknowledges the conversion results. Issuing a not acknowledge frees the bus allowing the master to generate a STOP or repeated START.

Applications Information

Power-On Reset

When power is first applied, internal power-on reset circuitry activates the MAX1069 in shutdown. When the internal reference is used, allow 12ms for the reference to settle when C_{REF} = 10µF and C_{REFADJ} = 0.1µF.

Automatic Shutdown

The MAX1069 automatic shutdown reduces the supply current to less than 0.6µA between conversions. The MAX1069 I²C-compatible interface is always active. When the MAX1069 receives a valid slave address the device powers up. The device is then powered down again when the conversion is complete. The automatic shutdown function does not change with internal or external reference. When the internal reference is chosen, the internal reference remains active between conversions unless internal reference shutdown is requested (see the *Internal Reference Shutdown* section).

Internal Reference Shutdown

The R/$\overline{W}$ bit of the slave address controls the MAX1069 internal reference shutdown. In external reference mode (REFADJ = AV_{DD}), R/$\overline{W}$ is a don't care. In internal reference mode, setting R/$\overline{W}$ = 1 places the device in normal operation and setting R/$\overline{W}$ = 0 prepares the internal reference for shutdown.

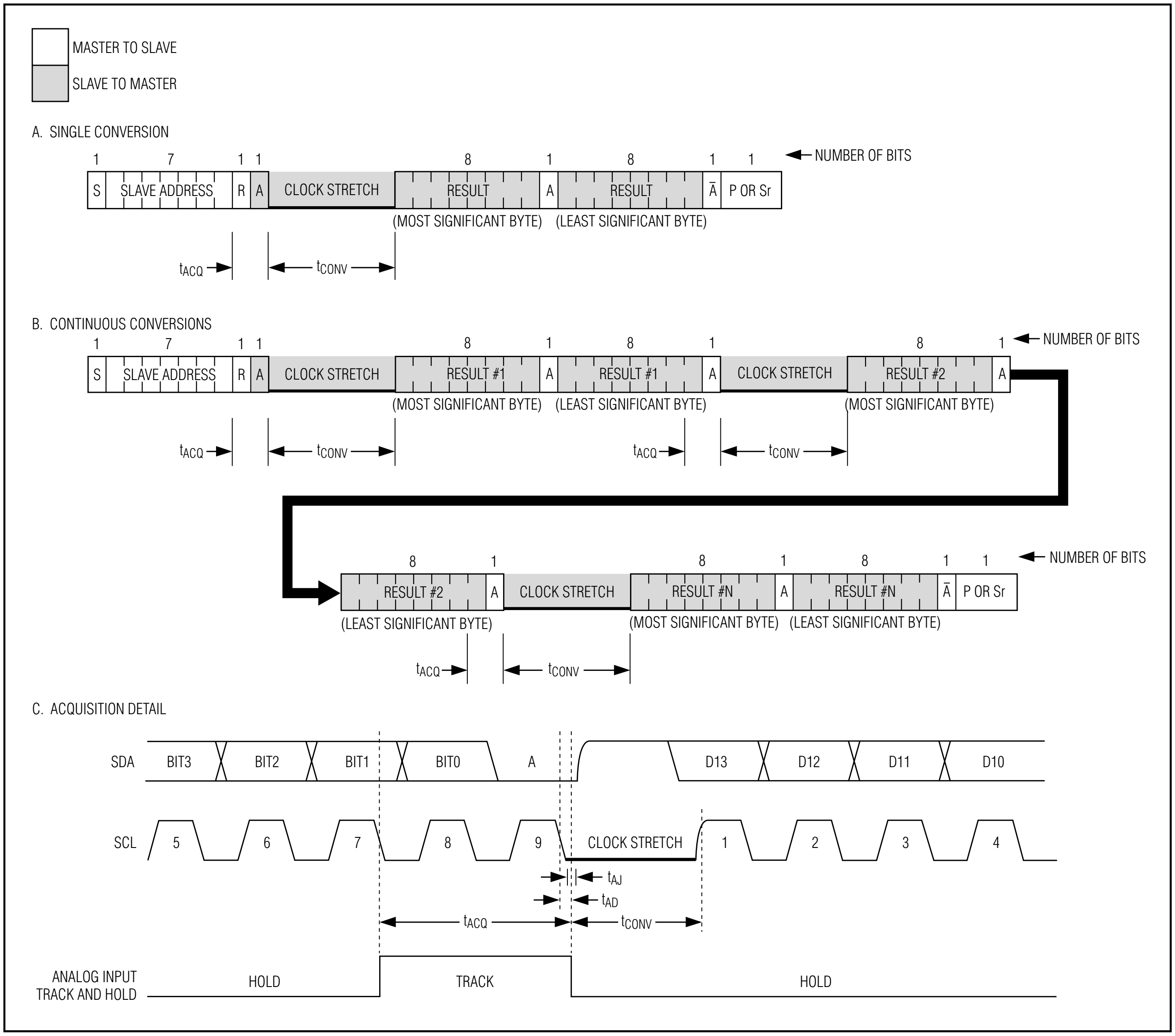


Figure 11. Read Cycle

If the internal reference is used and R/$\overline{W}$ = 0, shutdown occurs when the master issues a not-acknowledge bit while reading the conversion results. The internal reference and internal reference buffer are disabled during shutdown, reducing the analog supply current to less than 1µA.

A dummy conversion is required to power up the internal reference. The MAX1069 internal reference begins powering up from shutdown on the 9th falling edge of a valid address byte. Allow 12ms for the internal reference to settle before obtaining valid conversion results.

Reference Voltage

The MAX1069 provides an internal or accepts an external reference voltage. The ADC input range is from V_{AGNDS} to V_{REF} (see the *Transfer Function* section).

Internal Reference

The MAX1069 contains an internal 4.096V bandgap reference. This bandgap reference is connected to REFADJ through a 5kΩ resistor. Bypass REFADJ with a 0.1µF capacitor to AGND. The MAX1069 reference buffer has a unity gain to provide +4.096V at REF. Bypass REF with a 10µF capacitor to AGND when the internal reference is used (Figure 12).

The internal reference is adjustable to ±1.5% using the Figure 13 circuit.

External Reference

For external reference operation, disable the internal reference by connecting REFADJ to AV_{DD}. During conversion, an external reference at REF must deliver up to 100µA of DC load current and have an output impedance of less than 10Ω.

For optimal performance, buffer the reference through an op amp and bypass REF with a 10µF capacitor. Consider the MAX1069's equivalent input noise ($80µV_{RMS}$) when choosing a reference.

Transfer Function

The MAX1069 has a standard unipolar transfer function with a valid analog input voltage range from V_{AGNDS} to V_{REF}. Output data coding is binary with 1LSB = ($V_{REF}/2^N$) where 'N' is the number of bits (14). Code transitions occur halfway between successive-integer LSB values. Figure 14 shows the MAX1069 input/output (I/O) transfer function.

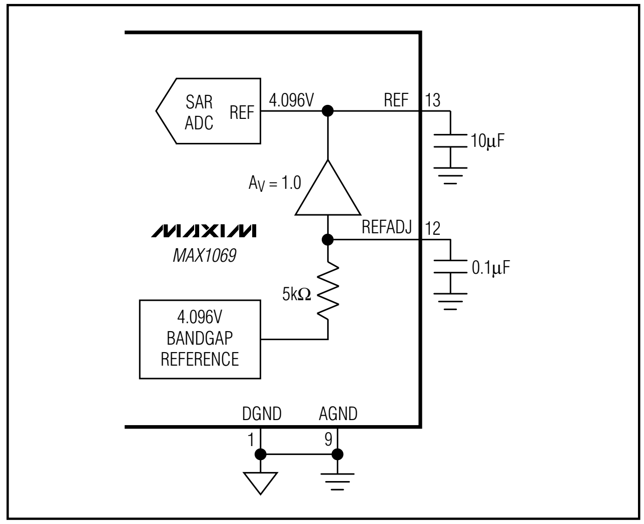


Figure 12. Internal Reference

Input Buffer

Most applications require an input buffer amplifier to achieve 14-bit accuracy. If the input signal is multiplexed, the input channel should be switched immediately after acquisition, rather than near the end of or

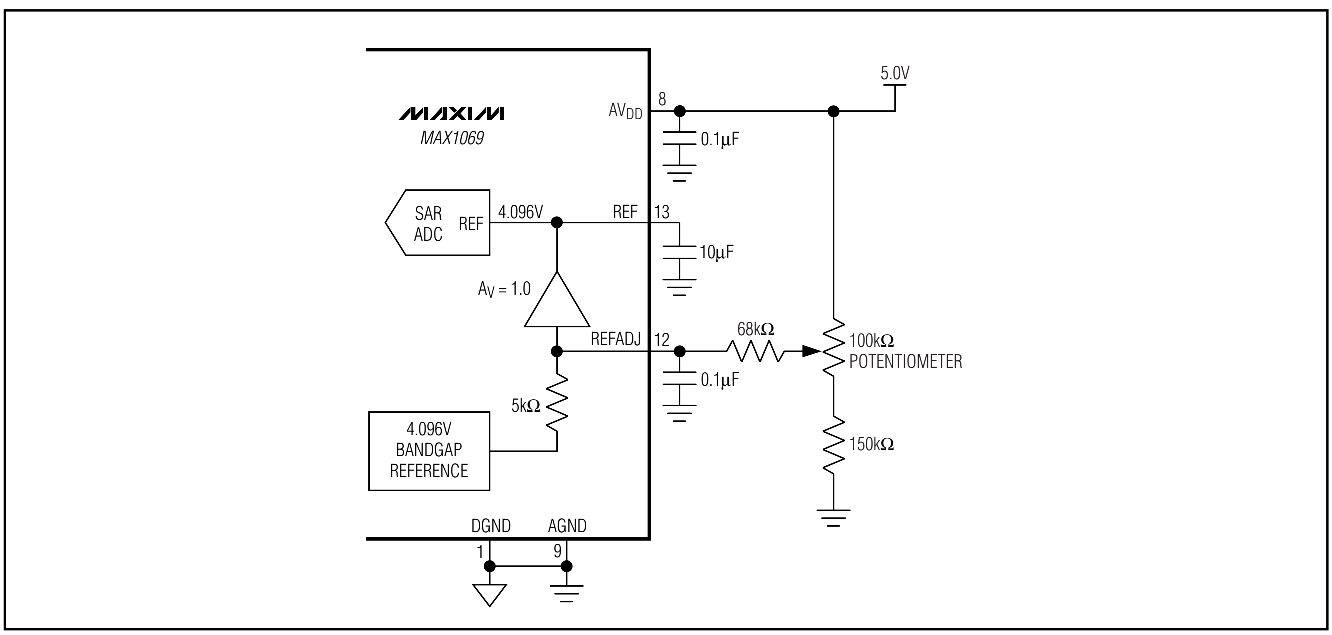


Figure 13. Adjusting the Internal Reference

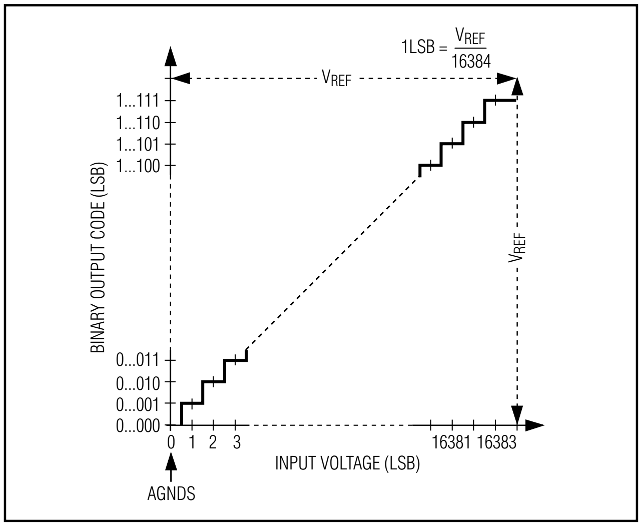


Figure 14. Unipolar Transfer Function

after a conversion. This allows more time for the input buffer amplifier to respond to a large step-change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time. At the beginning of acquisition, the internal sampling capacitor array connects to AIN (the amplifier output), causing some output disturbance.

Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the internal sampling capacitor with very little ripple. However, for AC use, AIN must be driven by a wideband buffer (at least 4MHz), which must be stable with the ADC's capacitive load (in parallel with any AIN bypass capacitor used) and also settle quickly. Refer to Maxim's website at www.maxim-ic.com for application notes on how to choose the optimum buffer amplifier for your ADC application.

Layout, Grounding, and Bypassing

Careful printed circuit (PC) layout is essential for the best system performance. Boards should have separate analog and digital ground planes and ensure that digital and analog signals are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the device package.

Figure 4 shows the recommended system ground connections. Establish an analog ground point at AGND and a digital ground point at DGND. Connect all analog grounds to the star analog ground. Connect the digital grounds to the star digital ground. Connect the digital ground plane to the analog ground plane at one point. For lowest-noise operation, make the ground return to the star ground's power-supply low impedance and make it as short as possible.

High-frequency noise in the AV_{DD} power supply degrades the ADC's high-speed comparator performance. Bypass AV_{DD} to AGND with a 0.1µF ceramic surface-mount capacitor. Make bypass capacitor connections as short as possible. If the power supply is very noisy, connect a 10Ω resistor in series with AV_{DD} and a 4.7µF capacitor from AV_{DD} to AGND to create a lowpass RC filter.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function once offset and gain errors have been nullified. The MAX1069 INL is measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples (Figure 11).

Aperture Delay

Aperture delay (t_{AD}) is the time from the falling edge of SCL to the instant when an actual sample is taken (Figure 11).

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = ((6.02 \times N) + 1.76)dB$$

In reality, noise sources besides quantization noise exist, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD(db) = 20 \times \log\left(\frac{Signal_{RMS}}{Noise_{RMS}}\right)$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the ADC's full-scale range, calculate the ENOB as follows:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the RMS sum ratio of the input signal's first five harmonics to the fundamental itself, expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{{V_2}^2 + {V_3}^2 + {V_4}^2 + {V_5}^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

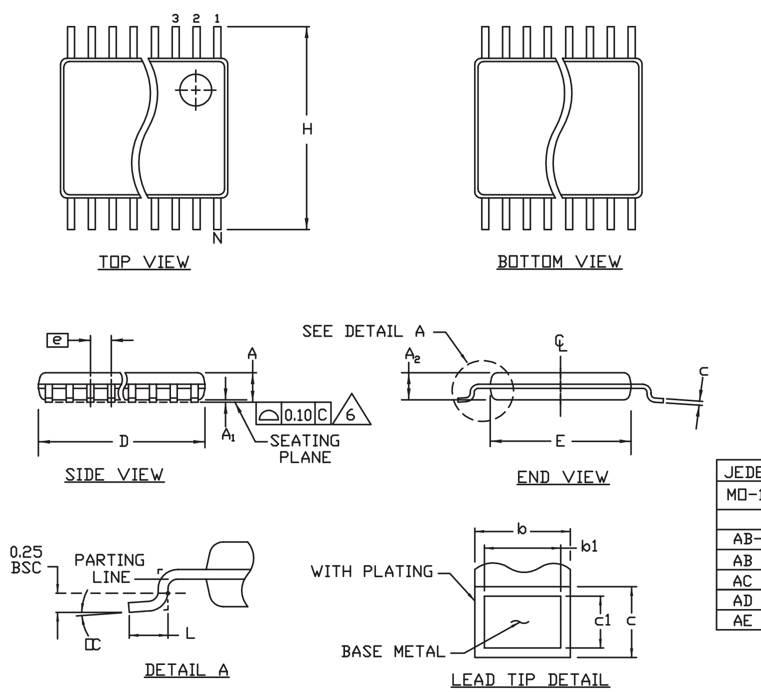
TRANSISTOR COUNT: 18,269
PROCESS: BiCMOS

58.6ksps, 14-Bit, 2-Wire Serial ADC in a 14-Pin TSSOP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1